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Frequency Response of C–V and G/ω-V Characteristics of Au/(Nanographite-doped PVP)/*n*-Si Structures

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ABSTRACT

This paper reports that frequency response on profile of C–V–*f* and G/ω–V–*f* characteristics of spin-coated nanographite (NG)-doped polyvinylpyrrolidone (PVP)/n-Si structures in a wide frequency (1 kHz–5 MHz) and voltage (± 3 V) ranges at room temperature. Hereby, the basic parameters of the structure such as diffusion potential (V_D), doping donor density (N_D), Fermi energy level (E_F), maximum electric field (E_m), depletion layer thickness (W_d), and barrier height (Φ_B) are derived by using the intercept and slope of C^{-2}–V–*f* plot for each frequency. Additionally, the energy density distribution of surface states (N_{ss}) and their relaxation time values (τ) are also attained from the conduction method and their values are found as 4.999×10^{12} eV^{-1} cm^{-2} and 2.92 μs at 0.452 eV, and 3.857×10^{12} eV^{-1} cm^{-2} and 164 μs at 0.625 eV, respectively. The lower N_{ss} values are the consequence of passivation effect of the used nanographite (NG)-PVP polymer interlayer. As a result, the polymer interlayer based nanographite (NG)-PVP is candidate instead of the widely used oxide/insulator layer for the purpose of decreasing the surface states or dislocations.

1 Introduction

Recently, metal–semiconductor (MS) structures have become very popular for scientists, engineers, and technology companies in line with the needs of growing electronic industry. Additionally, MS structures with an interfacial insulator, ferroelectric and organic layer for developing new electronic devices are very important for fast switching applications with low voltage drop in the radio frequency, microwave and terahertz power and communication electronics [1–6]. Among these interfacial layer materials, organics/polymers have some advantages like low cost, flexibility, easy grown method, low-

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temperature production, high strength, low molecular weight compared to the insulators. In traditional applications, the interfacial layer is generally an insulator/oxide layer like SiO_2 and SnO_2 which are called as metal-oxide/insulator-semiconductor (MOS or MIS) structures [7, 8]. In the MS structure with an interfacial layer, the metal is isolated from the semiconductor thanks to the used interfacial layer and it has a continuous distribution of interface traps/surface states (D_{it}/N_{ss}) between semiconductor and interlayer. When the MOS/MIS type structures have series resistance (R_s) and surface states (N_{ss}), their electrical and dielectric behaviors considerably differ from the ideal case especially at low and intermediate frequencies in depletion and inversion regions [9, 10]. Therefore, recent applications show us that the interlayer of the MS structures can be chosen as a polymer or its some composites as an interfacial layer instead of conventional insulators by prepared traditional methods such as thermal or wed oxidation. Because, an organic/polymer interfacial layer, due to their easy synthesis and applications, has become a cost-effective solution to decrease surface states which are located between it and semiconductor. So that, they can be deposited by dip coating, spin coating, spray coating, electrospinning, and sol–gel techniques which are very low cost. On account of their nature, synthesis of the polymer films is easy, and the material diversity is quite extensive [11, 12].

The surface quality of the thin film devices always plays a significant role on the performance and reliability of the devices regardless of the types of semiconductor devices such as light-emitting diodes (LEDs), laser diodes (LDs), transistors, switching diodes or other semiconductor devices combined with different types of layers such as passivation layers, ohmic contacts, gate oxides, Schottky contacts/diodes (SDs), optical coatings or epitaxial layers. This is the most challenging point of the semiconductor industry and research and development processes. Because, recently, the main scientific and technical problems of MS structures with and without an interlayer are relevant to the increase in the performance of them in respect of decrease of N_{ss}, R_s, leakage current, barrier in-homogeneities. Therefore, many scientists struggle to eliminate the surface effects of deposited or grown layers on device performance and secondly, to get more reliable devices.

Especially, the high dielectric polymer interlayer with some metals or grapheme-doped have very high insulating features blocking diffusion currents and reactions between M-S layers. Also, N_{ss} and dislocations are treated by the polymeric passivation. Because, low dielectric materials like SiO_2 cannot be enough to block current leakages and cause more N_{ss} by passivating dangling bonds of semiconductor surface. These malfunctions affect the performance and reliability of devices. To avoid these cases, researchers spend more and more effort to enhance the performance and reliability of semiconductor devices with the use of low-cost materials and methods. Among polymers, especially the polyvinyl alcohol (PVA) and polyvinylpyrrolidone (PVP) The polymer materials used as an interlayer at M/S interface due to easy soluble in water, low scattering loss, good charge storage capacity, high dielectric strength, and dopant dependent electrical properties [9, 13]. Therefore, nowadays, researchers have studied on doping the layer with substances such as metals, alloys, semiconductor nanoparticles, allotropes of carbon to enhance their conductivity [14, 15]. Also polymer materials, in scope of surface-to-volume ratio, mechanical strength, capacitive properties, life length and producibility features, become prominent among other materials [16].

In order to benefit from the superior features, allotropes of carbon have been extensively studied by researchers all around the world. Many forms of carbon such as diamond, fullerene, graphene, graphite become more and more popular due to electrical, mechanical, tribological and thermal properties [17–19]. As an allotrope of carbon, graphite has many stacked two-dimensional carbon–carbon bonded layers named graphene resulting strong Van der Waals forces, on c-axis [20]. The interest on the excellent electronic properties of graphene has resulted to research new materials related. Polymers combined with nanoparticles, as being polymer nanocomposites, have new great functional properties for instance electrical, thermal, luminous, antibacterial characteristics as well as mechanical properties [21]. Doping polymers with NG helps us not only to enhance the electrical, thermal properties but also to design and tune the properties, purposefully. NG particles, owing to the mechanical strength, great electrical conductivity, easy synthesis etc., are extensively used as an alternative to carbon nanotubes or nanofibers (CNT/CNF) [22, 23].

The existence of N_{ss} and R_s leads to be deviated from the ideal case of the MS structures. N_{ss} are

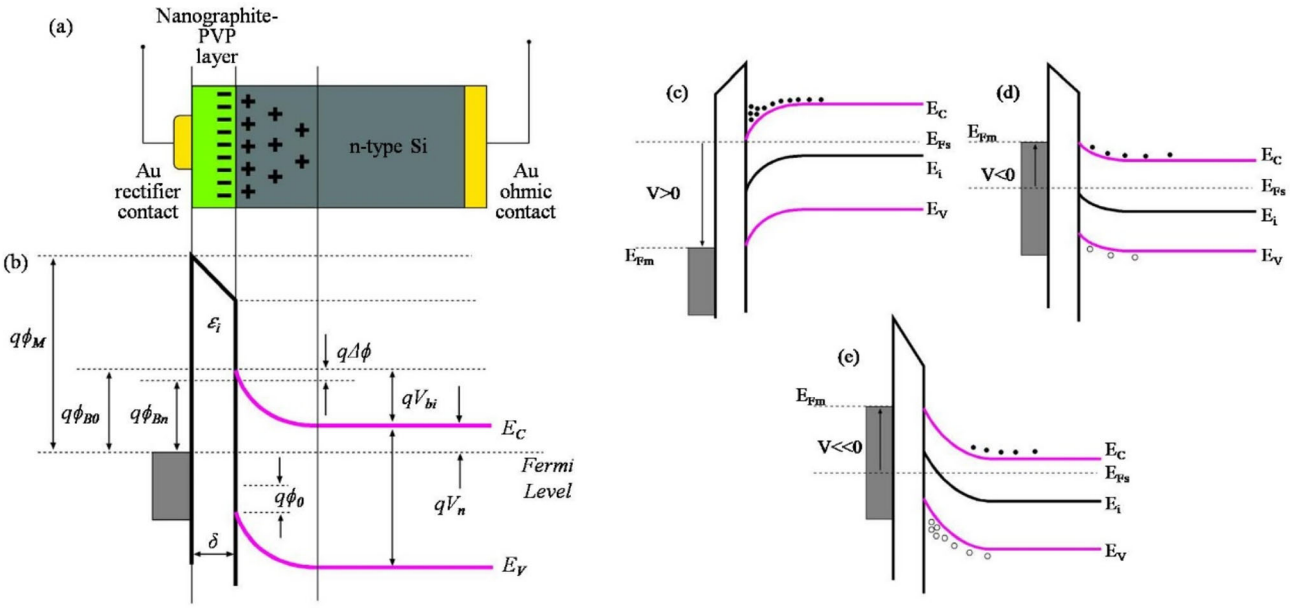

Fig. 1 **a** Illustration and **b** the energy band formation of the device, **c** accumulation, **d** depletion, and **e** inversion cases of the Au/(nanographite-doped PVP)/n-Si structure with different bias polarizations

usually resulted from surface structure, lattice disorder, surface preparation, and impurities in semiconductor, but R_s is resulted from the ohmic and back contacts, probe wires to the gate, and bulk resistivity [9]. The used a high dielectric interlayer such as NG-doped PVP can utilize the MIS/MPS structures in scope of reliability and performance [9, 24–31]. These traps yield an excess C and G the measured of them at low frequencies [25, 32–36].

In this study, NG-doped PVP thin films were fabricated and used as an interlayer for MS structures. The (C–V–f and G/ω–V–f) measurements were done in a wide frequency (1 kHz–5 MHz) and voltage (± 3 V) ranges at room temperature. With the obtained data, C^{-2}–V–f plots were generated and using the linear fit to those plots, some characteristic parameters such as Schottky barrier height (Φ_B), donor density (N_D), Fermi energy level (E_F), maximum electric field (E_m), depletion layer thickness (W_d) were derived.

2 Experimental details

Experimentally, Au/n-Si type structures with NG-PVP thin film polymers were produced to investigate the frequency response of C–V–f and G/ω–V–f characteristics of them. Before the production process, firstly, n-Si wafer with 1–10 Ω.cm resistivity was subjected to chemical cleaning processes in ammonium-peroxide for 1 min to get rid of native-oxide and organic residuals on the surface. After that, it was cleaned in the H_2SO_4:H_2O_2:H_2O with 3:1:1 and HCl: H_2O with 1:1 volume ratio for 1 min, and then it was dried by dry nitrogen gas (N_2) to prevent any oxidation on the surface. Immediately, it was transferred to high-vacuum metallization system and then 200-nm-thick highly pure gold (Au, 99.999%) was evaporated to whole backside of n-Si wafer with thermal evaporation method. To create high quality or low-resistive ohmic contact, n-Si/Au wafer was annealed at 550 ºC for 5 min. After that, the prepared NG-PVP solution was grown onto polished surface of n-type Si wafer by using spin coating method. Finally, high-pure Au dots with 0.5 mm radius are also deposited onto the NG-PVP polymer film layer with the same deposition method. The C–V–f and G/ω–V–f characteristics of the structures with measuring the impedance spectroscopy were obtained using HP 4192A LF impedance analyzer via a microcomputer IEEE-488 AC/DC converter card. Thus, the production and measurement process of the structures was completed.

An illustration of the fabricated Au/(nanographite-doped PVP)/n-Si structure and the energy band

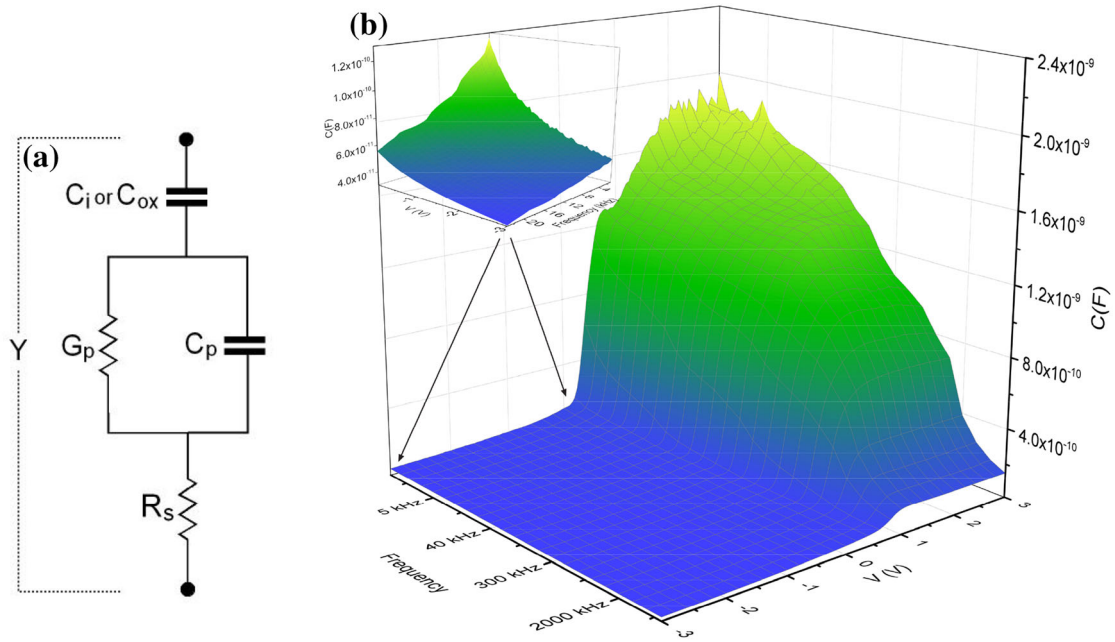

Fig. 2 **a** The equivalent circuit of nanographite-doped PVP/n-Si MIS structure, **b** The C–V–*f* characteristics of spin-coated nanographite-doped PVP/*n*-Si structures

formation at accumulation, depletion, and inversion cases was given in Fig. 1, respectively.

As shown in Fig. 1b, for n-type semiconductor, electrons from the conduction band (E_C) which have higher energy than metal electrons flow into to the metal until the Fermi energy (E_F) of semiconductor and metal is brought into coincidence. Thus, the electron concentration near the boundary of semiconductor side declines and then in thermal equilibrium, E_F remains constant and in this case the rate of electrons crossing over the formed barrier from the semiconductor into metal is balanced by the rate of electrons across the barrier in the opposite direction and no net current flows. When these structures are biased with positive and negative biases, usually three cases may exist at the semiconductor surface which are accumulation, depletion, and inversion regions [35, 38]. Therefore, the energy bands or C–V plots are classified accumulation, depletion, and inverse regions, but sometimes C–V plot can be classified in five regions which are strong accumulation, weak accumulation, depletion, weak inversion and strong inversion. In the ideal case both in the strong accumulation and inversion region, the value of C becomes almost independent of voltage, but it was more changed with applied bias voltage especially in depletion region rather than weak accumulation and inversion regions.

3 Results and discussion

There are many studies, suggesting different ways of characterization for the energy or voltage-dependent profile of surface states (N_{ss}) [24, 25, 35, 37]. The technique giving the most accurate results among these ways is admittance/conductance technique revealed by Nicollian and Goetzberger [8, 24, 35]. This method requires many C–V and G/ω–V measurement in wide frequency and applied bias voltage ranges. According to them, the relationship between the admittance or impedance $(Y = (1/Z) = G + j\omega C)$ and N_{ss} of the structures can be determined from these measurements.

Figure 2a illustrates the equivalent circuit diagram for Au/Nanographite-PVP/n-Si MIS structure. Figures 2b and3. indicate the *C–V–f* and*G/ω–V–f* behavior of the Au/Nanographite-PVP/*n*-Si type structure measured for the frequencies from 1 kHz to 5 MHz, voltage of ± 3 V and the peak to peak value of AC signal was kept at 50 mV, at room temperature. In addition, these figures have inversion, depletion and accumulation regions. It is obvious that both C and G/ω are strong function of frequency and voltage. But, the changes in the C and G/ω become more prominent in the depletion and accumulation regions at low and intermediate frequency. Because, the surface states can easily trace an external alternating

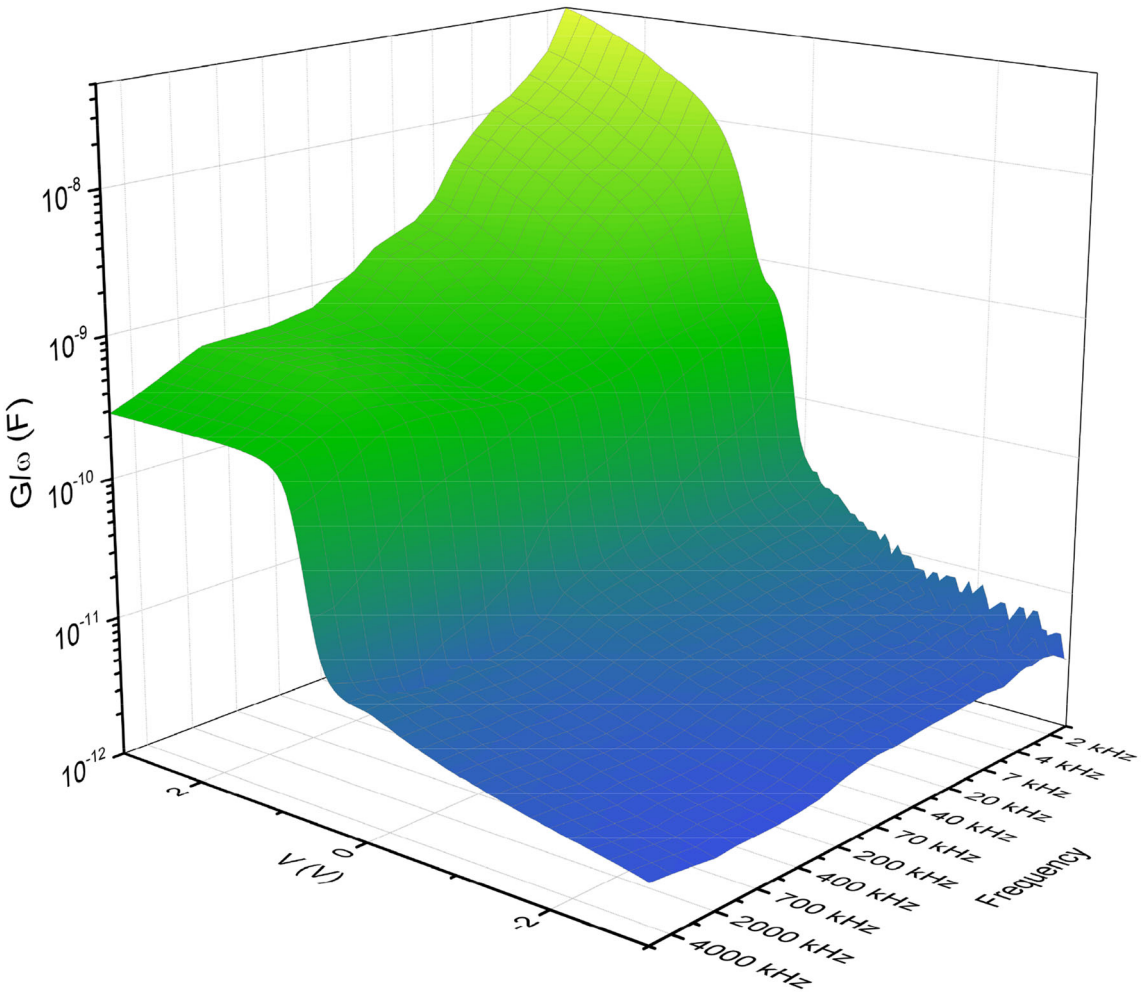

Fig. 3 The G/ω–V–f characteristics of spin-coated nanographite-doped PVP/n-Si structures

current (AC) signal at low frequencies and generate an excess capacitance and conductance to the measured real values of them. The observed higher values of C and G/ω at low and moderate frequencies are the resulted from N_{ss} which are equilibrium with the semiconductor and their relaxation time (τ). In other respects, the observed discrepancies in C and G/ω at accumulation region are resulted from the existence of R_s and polymer layer rather than N_{ss}. In other words, while N_{ss} are prominent both in the inversion and depletion regions, R_s is prominent only at accumulation region. The N_{ss} traps induce levels located in forbidden band gap is usually resulting from the discontinuities of the periodic lattice structure at surface, some organic impurities in the laboratory condition and vacancies. But, the existence of the R_s is usually resulting from the back ohmic (on the n-Si wafer) and front rectifier contacts (on the (nanographite-PVP) polymer layer), non-uniformity of the doping of donor or acceptor atoms, crystal dislocations and impurities.

The existence of R_s can cause deviation in the ideal C–V–f and G/ω–V–f plots especially at accumulation region of the structures. Thereby, the voltage-dependent R_s profile of Au/nanographite-PVP)/n-Si type structure was extracted from the acquired C and G data for each frequency. Then, the R_s vs. V plot of the structure was generated by using Nicollian and Goetzberger method as described in Eq. 1 and given in Fig. 4. [35]. Herein, the R_s vs. V curves have a characteristic peak in the region of 0–1 V for each frequency. While the magnitude of peak declines and its position goes to the higher positive voltage, with increasing frequency.

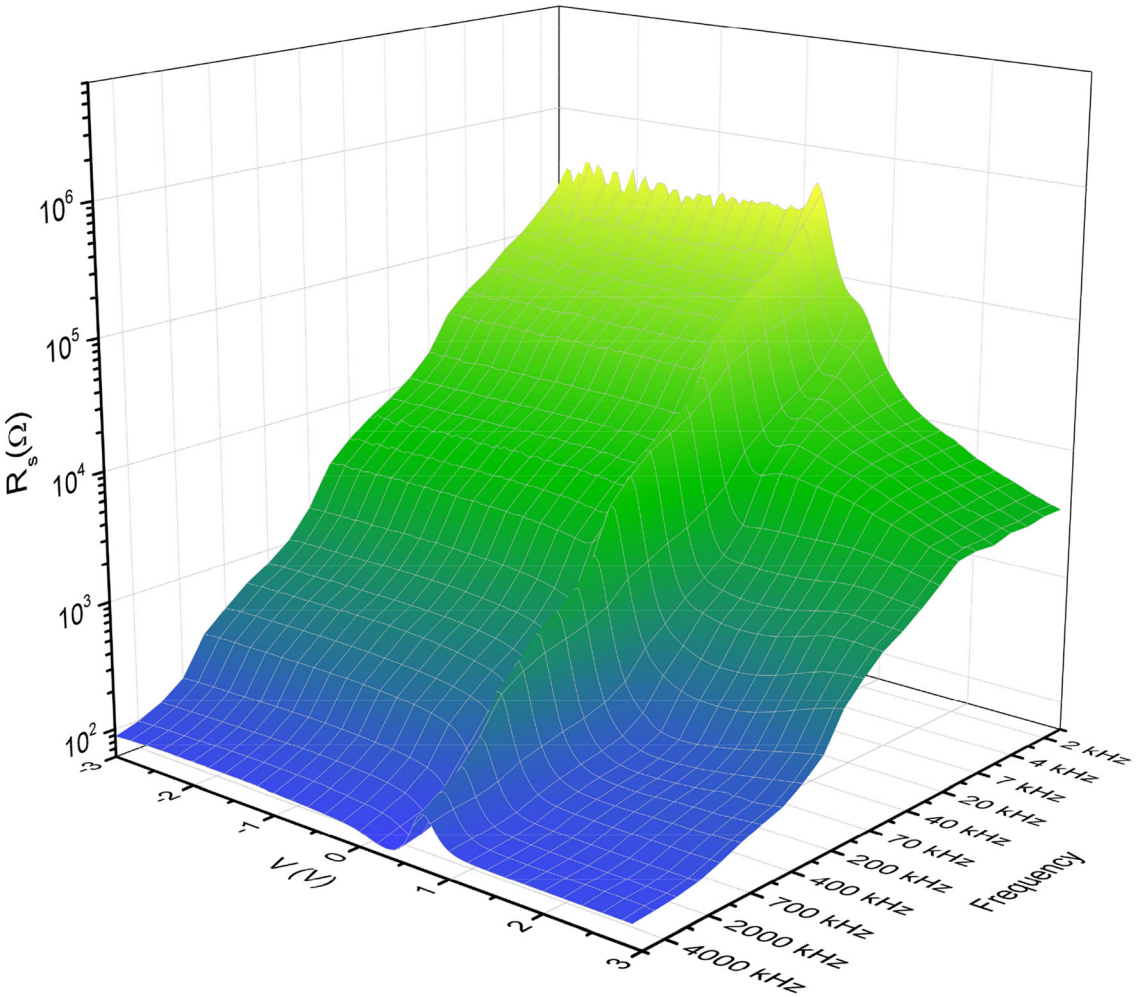

Fig. 4 The R_s-V-f characteristics of spin-coated nanographite-doped PVP/n-Si structures

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})} \quad (1)$$

According to Fig. 4, it is quite obvious that the R_s depends on frequency and voltage changing from region to region, due to a special distribution of N_{ss} between polymer interlayer and n-Si in the forbidden band gap. On the other hand, the real R_s value accounts for the strong accumulation region according to Nicollian and Goetzberger [35].

In a wide frequency range, the depletion layer capacitance related with reverse bias voltage (V_R) is expressed as below:

$$\frac{1}{C^2} = \frac{2(V_o - kT/q + V_R)}{q\varepsilon_S\varepsilon_O A^2 N_D} \quad (2)$$

In Eq. 2, ε_s is the permittivity of a semiconductor, equals to 11.68 for Si, N_D is doping concentration of donor atoms, and A is the rectifier contact area. To determine the basic electrical parameters of the structure such as N_D, Fermi energy (E_F), depletion layer width (W_d) and barrier height (Φ_B) as function of frequency, C^{-2}–V plots were obtained and used for calculation for each frequency. Thus, the reverse biased C^{-2}–V–f plots are expressed in Fig. 5. Herein, C^{-2} vs. V plots have a quite linear behavior in voltage boundaries of (− 1.5)–(0) V.

The value of intercept voltage (V_0) and N_D were calculated by using the intercept and slope of the C^{-2}–V plot for each frequency. Subsequently, the Fermi energy level, E_F and barrier height of C-V measurement, $\Phi_{B(C\text{-}V)}$values of the structure were obtained using the Eqs. 3and4b, respectively [38].

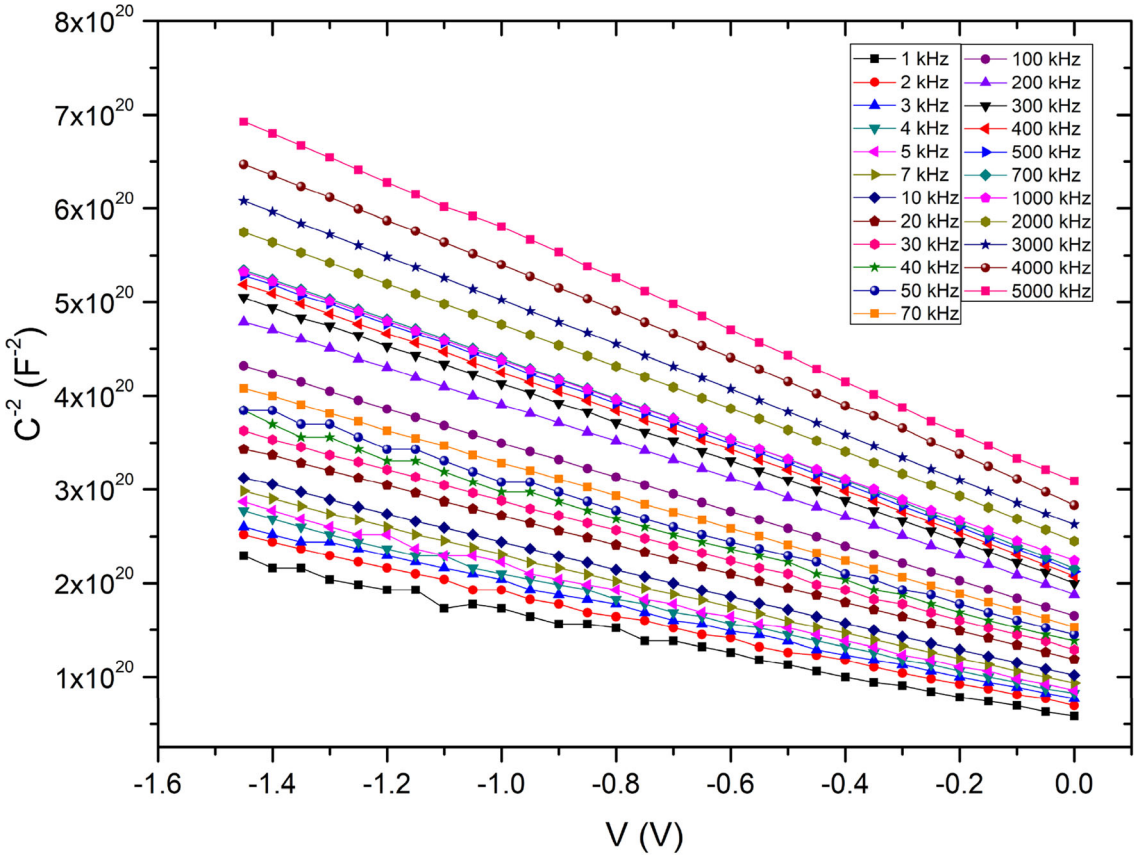

Fig. 5 The C^{-2}–V–f characteristics of spin-coated nanographite-doped PVP/n-Si structures

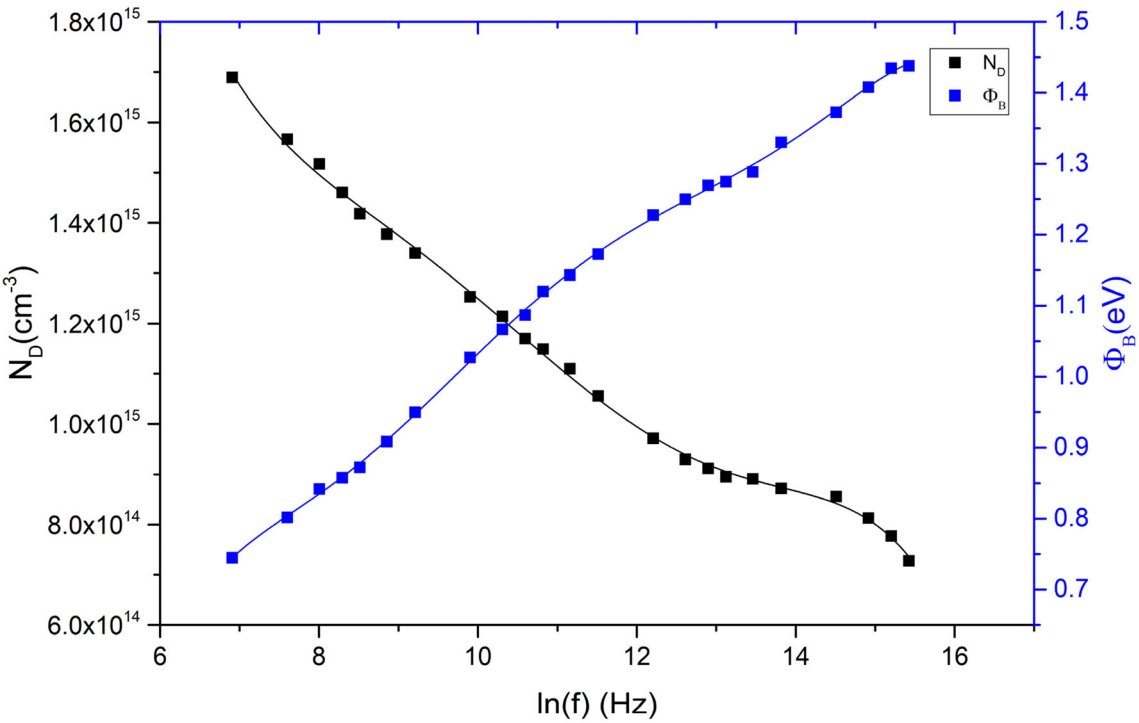

Fig. 6 N_D and Φ_B versus ln(f) plots of the structure

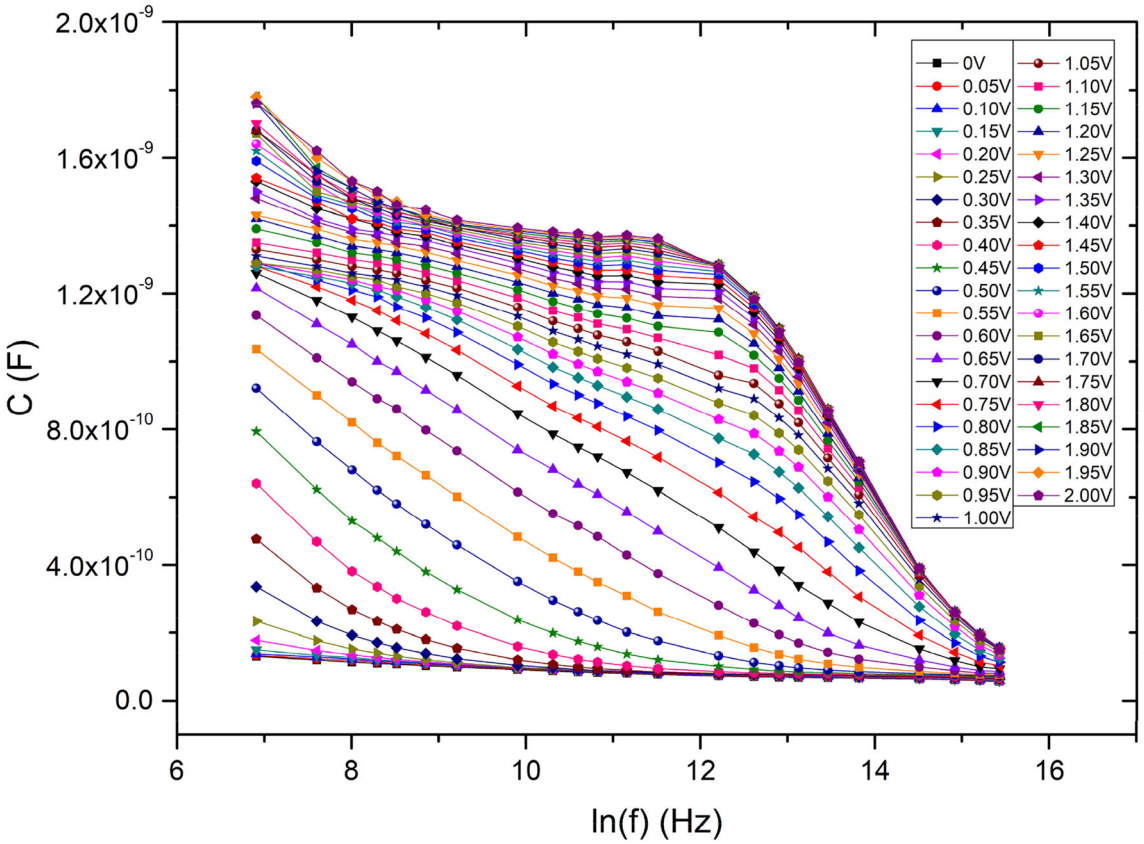

Fig. 7 The *C-ln(f)* plots of the structure at distinct applied voltages

$$E_F = \frac{kT}{q}\ln\left(\frac{N_C}{N_D}\right) \tag{3}$$

$$\phi_B = V_O + kT/q + E_F - \Delta\phi_B \tag{4a}$$

$$\phi_{B(C-V)} = c_2 V_O + kT/q + E_F - \Delta\phi_B \tag{4b}$$

In Eqs. 3and 4, N_C is the density of states at conduction band, kT/q is thermal energy, $\Delta\Phi_B$ is the image force lowering, c_2 is the ratio of experimental and theoretical values of N_D. The existence of an interfacial layer, N_{ss} and R_s leads to a large intercept voltage as can be seen in Table. While the N_{ss} are effective at low frequencies, R_s effective at high frequencies [24, 38]. In this case the value of ϕ_B becomes higher than forbidden bandgap (E_g) of semiconductor especially at high frequency. Therefore, the value of ϕ_B can be modified by using c_2 factor which is the ratio of the experimental and the theoretical values of N_D. The value of N_D and W_d were also calculated from Eq. 5(a) and 5(b)using the value of slope ($tan\theta$) and intercept voltage ($V_o = V_D - kT/q$), respectively.

$$N_D = 2/\left(q\varepsilon_s\varepsilon_o A^2 \tan\theta\right) \tag{5a}$$

$$W_d = \left(2\varepsilon_s V_d/qN_D\right)^{1/2} \tag{5b}$$

The V_D, N_D, E_F, E_m, W_d, c_2,$\Delta\Phi_B$, and $\Phi_{B(C\text{-}V)}$ values of the structure are tabulated in Table 1.

As stated in Table 1 and Fig. 6; while the W_d and $\Phi_B$values increase with increasing frequency the N_D value decreases as almost exponentially. The N_D, W_d, Φ_B values change in the ranges of 1.689×10^{15}–7.275×10^{14} cm^{-3}, 0.629–1.457 µm, and 0.745–1.438 eV with increasing frequency, respectively. The surface states and surface charges are able to keep up with the alternating or AC signal at low intermediate frequency and so, generate an excess C and G to the measured values of them. In other words, the intercept point of the C^{-2}–V–f plots increases with increasing frequency.

Since N_{ss} exist between the insulator/polymer interlayer and semiconductor, MIS/MOS type structures deviate from the ideal case. These traps/states within the forbidden band gap of the semiconductor exist owing to the discontinuity of the lattice

Table 1 The empirical values of V_o, N_D, E_f, E_m, W_d, V_D, $\Delta\Phi_B$, c_2,n, $\Phi_{B(C-V)}$ and R_s according to the frequency

f (kHz)	V_o (V)	N_D (cm^{-3})	E_f (eV)	E_m (V/cm)	W_d (μm)	V_D (eV)	$\Delta\Phi_B$ (meV)	Φ_B (eV)	c_2	n = 1/c_2	$\Phi_{B(C\text{-}V)}$ (eV)	R_s (at 3 V) (Ω)
1	0.486	1.689×10^{15}	0.248	15861.46	0.629	0.512	13.910	0.745	0.784	1.276	0.640	3340.71
2	0.541	1.566×10^{15}	0.250	16116.64	0.687	0.567	14.021	0.802	0.727	1.376	0.654	3360.06
3	0.580	1.518×10^{15}	0.250	16429.32	0.722	0.606	14.157	0.842	0.704	1.420	0.670	3186.82
4	0.595	1.460×10^{15}	0.251	16324.73	0.745	0.621	14.112	0.858	0.678	1.476	0.666	3244.84
5	0.609	1.418×10^{15}	0.252	16272.63	0.765	0.635	14.089	0.873	0.658	1.520	0.664	2951.15
7	0.645	1.378×10^{15}	0.253	16496.73	0.797	0.671	14.186	0.908	0.639	1.564	0.676	3054.42
10	0.686	1.340×10^{15}	0.254	16774.91	0.833	0.711	14.305	0.950	0.622	1.609	0.690	2932.39
20	0.761	1.253×10^{15}	0.255	17097.96	0.906	0.787	14.442	1.027	0.582	1.720	0.709	2192.61
30	0.800	1.214×10^{15}	0.256	17251.23	0.942	0.826	14.506	1.067	0.563	1.775	0.717	1670.46
40	0.819	1.170×10^{15}	0.257	17139.43	0.971	0.845	14.459	1.087	0.543	1.842	0.712	1300.40
50	0.852	1.149×10^{15}	0.258	17323.26	0.999	0.878	14.537	1.120	0.533	1.875	0.722	1076.86
700	0.874	1.110×10^{15}	0.258	17244.19	1.029	0.900	14.504	1.143	0.515	1.942	0.719	792.46
100	0.902	1.056×10^{15}	0.260	17083.28	1.071	0.928	14.436	1.172	0.490	2.041	0.712	548.66
200	0.955	9.712×10^{14}	0.262	16858.61	1.148	0.981	14.340	1.228	0.451	2.219	0.703	290.28
300	0.976	9.294×10^{14}	0.263	16672.62	1.186	1.002	14.261	1.250	0.431	2.319	0.695	214.05
400	0.995	9.119×10^{14}	0.264	16677.21	1.209	1.021	14.263	1.270	0.423	2.363	0.695	170.18
500	1.000	8.951×10^{14}	0.264	16561.71	1.223	1.026	14.214	1.275	0.415	2.407	0.690	151.34
700	1.014	8.910×10^{14}	0.264	16636.99	1.234	1.040	14.246	1.289	0.413	2.419	0.694	132.78
1000	1.056	9.119×10^{14}	0.264	17180.93	1.245	1.082	14.477	1.330	0.423	2.363	0.721	113.45
2000	1.097	8.557×10^{14}	0.265	16959.34	1.309	1.123	14.383	1.373	0.397	2.518	0.711	99.39
3000	1.100	8.127×10^{14}	0.267	16554.46	1.345	1.126	14.211	1.408	0.377	2.652	0.692	92.67
4000	1.156	7.770×10^{14}	0.268	16589.91	1.409	1.182	14.226	1.434	0.361	2.774	0.695	89.22
5000	1.157	7.275×10^{14}	0.269	16062.13	1.457	1.183	13.998	1.438	0.338	2.962	0.671	86.95

structure at the surface of the semiconductor [39–45]. The charges at these traps/states are quite effective both on the C-V and G-V characteristics of the structures and respond differently to the external AC signal. There are many methods to determine the distribution of N_{ss} as function of voltage or energy such as high-low capacitance, admittance/conductance, and Hill-Coleman methods [24, 35, 36]. Through them, the most proper method is the admittance method proposed by Nicollian and Brews [24, 35] which requires a series of *C–f* and *G/ω–f* plots for distinct applied voltages. Therefore, both the *C–ln (f)* and *G/ω–ln(f)* plots of the structure for different bias voltages are given in Figs. 7. and 8, respectively.

All these results show that during the fabrication processes of MS structures with and without insulator or polymer interfacial layer, many surface states (N_{ss}) and dislocations may occur in the forbidden band gap of semiconductor at metal–semiconductor interface. They are generally resulted from defects such as dangling bonds and some disorders in the crystal lattice, and doping donor or acceptor atoms. N_{ss} and polarization effects can be minimized by (1) sample fabrication and (2) performing measurements at enough high frequencies (f ≥ 500 kHz) so that the effect of them can be neglected. Because, at low frequencies, the charges at these states can keep up with the ac signal and yield both an excess capacitance and conductance to the measured real values of them. But, at high frequencies, these states cannot have any considerable contribution to the C and G/ω, since their relaxation/life times (τ) are too long to permit the charge to move in and out of the N_{ss} in response to ac signal [3–5, 8, 35]. Therefore, these states are more effective on the C/G-V plots especially in depletion and inversion regions. Thus, the obtained experimental values of N_D, Φ_B, and W_d, and from the reverse bias C^{-2} vs V plots become dependent of frequency as can be seen in Table 1. Because both the intercept points and slopes of the C^{-2} vs V plots change depending on interfacial layer, these states, and their lifetime. The decrease of N_{ss} at high frequencies leads to an increase in the intercept point

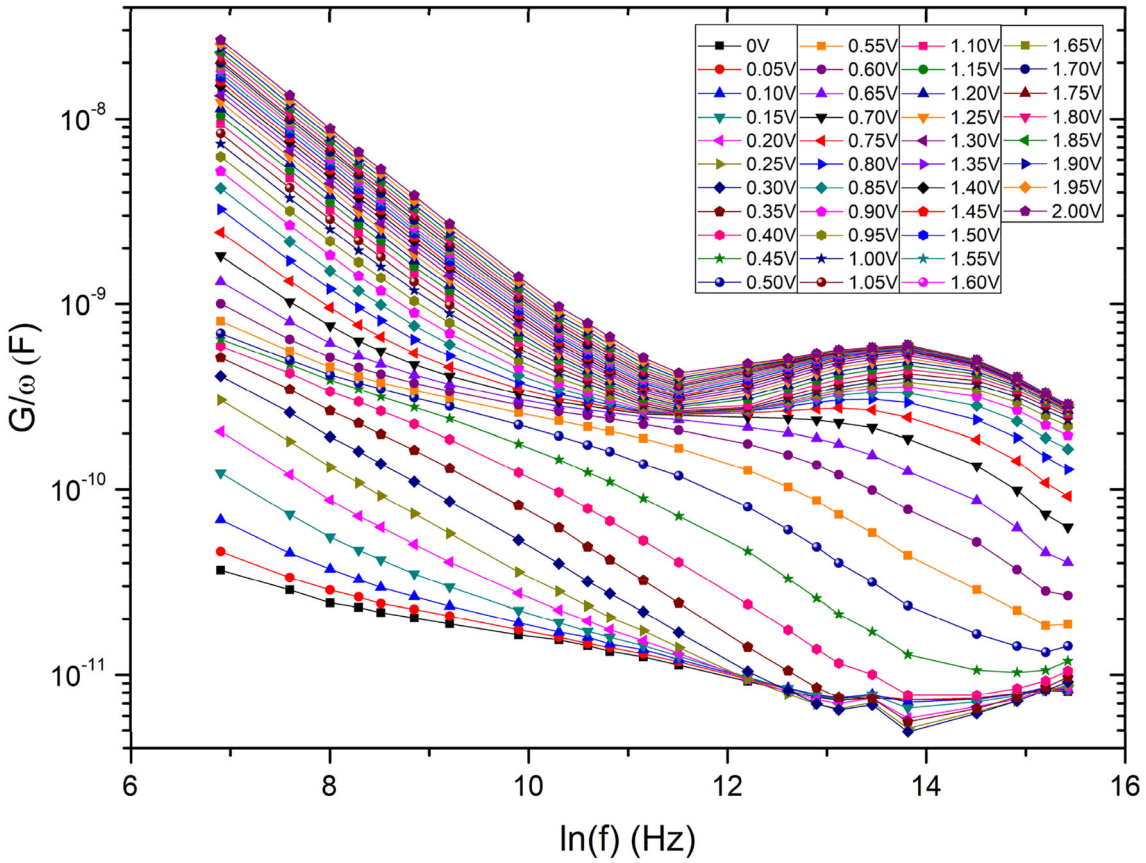

Fig. 8 The G/ω-$ln(f)$ plots of the structure at distinct applied voltages

(voltage-axis) and also barrier height, but decrease of the N_D or increase in W_d can be seen in Eq. 5b.

According to Nicollian and Brews, the parallel conductance (G_p/ω) values are given in Figs. 7. and 8 are calculated by using Eq. 6[24, 35]:

$$G_p/\omega = \frac{\omega C_m C_i^2}{G_m^2 + \omega^2 (Ci - C_m)^2} = \frac{qNss}{2\omega\tau} \ln[1 + (\omega\tau)^2] \quad (6)$$

Here, C_m and G_m are the measured capacitance and conductance values at any bias voltage, ω is the angular frequency, τ is the relaxation time of the surface states, and C_i the interfacial layer capacitance.

As located in Figs. 7and8, both C and G/ω values decrease with the increase of the frequency for nearly each bias voltage. But, the changes in the C and G/ω are notably high especially at low frequencies. Additionally, the G_p/ω vs $ln(f)$ plots in voltage range of 0.65–3.00 V by 50 mV steps are given in Fig. 9. There is a distinctive peak for each bias voltage and their positions shift towards higher frequency with the increase of applied bias voltage. In order to extract the values of N_{ss} and τ as function of energy the value of voltage was converted to energy (E_c-E_{ss}). The value of (E_c-E_{ss}) was derived from the forward bias I-V data of the Au/(NG-doped PVP)/n-Si structure (it has not given here) by considering voltage-dependent ideality factor (n(V)) and barrier height [ϕ_B(V)] as given following equations [37]:

$$n(V) = \frac{qV}{kT.Ln(I/I_o)} = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \quad (7a)$$

$$\Phi_e = \Phi_{Bo} + \alpha\,(V) = \Phi_{Bo} + \left(1 - \frac{1}{n(V)}\right)V \quad (7b)$$

In Eq. 7b, α is equal to $d\Phi_e/dV$ which is given by 1–1/n(V), ε_i is the permittivity of interlayer. Thus, the (E_c-E_{ss}) was estimated considering the bottom of E_c using the following relation [37].

$$E_c - E_{ss} = q(\phi_e - V) \quad (7c)$$

Thus, the value of (E_c—E_{ss}) was obtained for each voltage in Fig. 9 (0.65–3.0 V).

According to conductance method, the peak value of G_p/ω vs $ln(f)$ plot corresponds to $\omega\tau$ which is equal

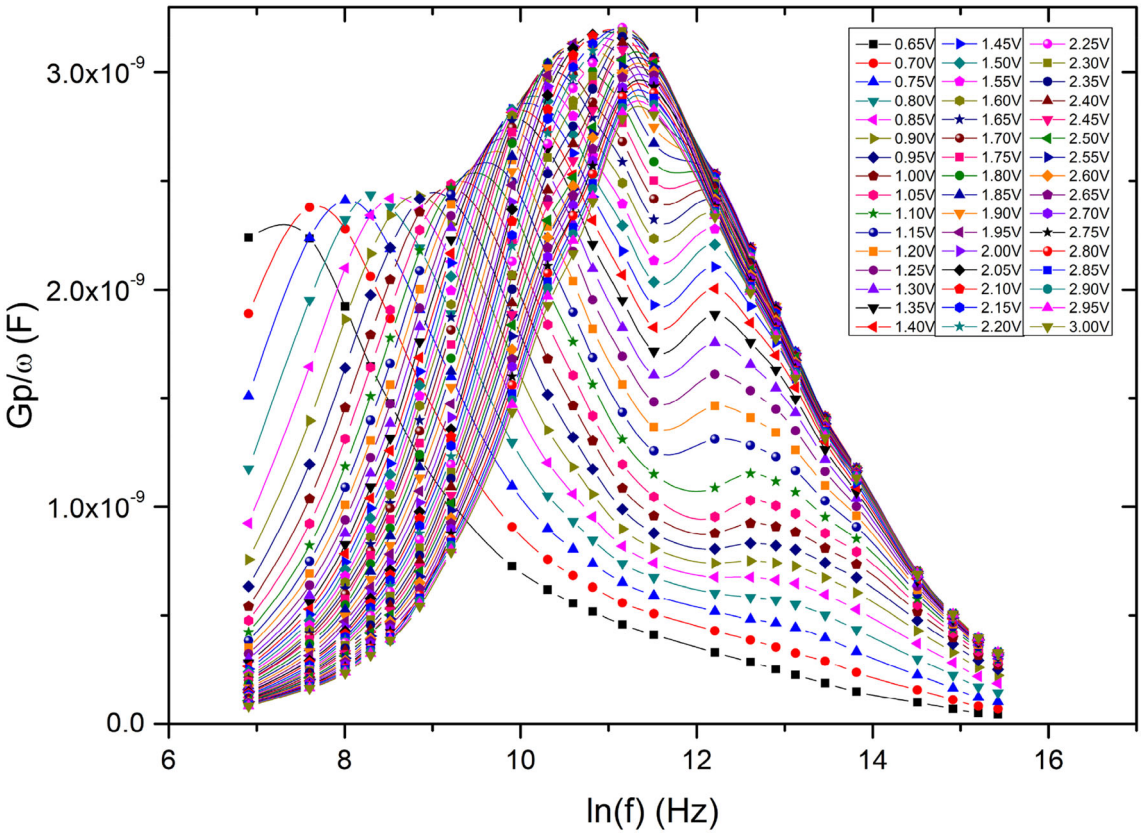

Fig. 9 The Parallel Conductance versus frequency plots, G_p/ω-ln(f), of the structure at various applied voltages

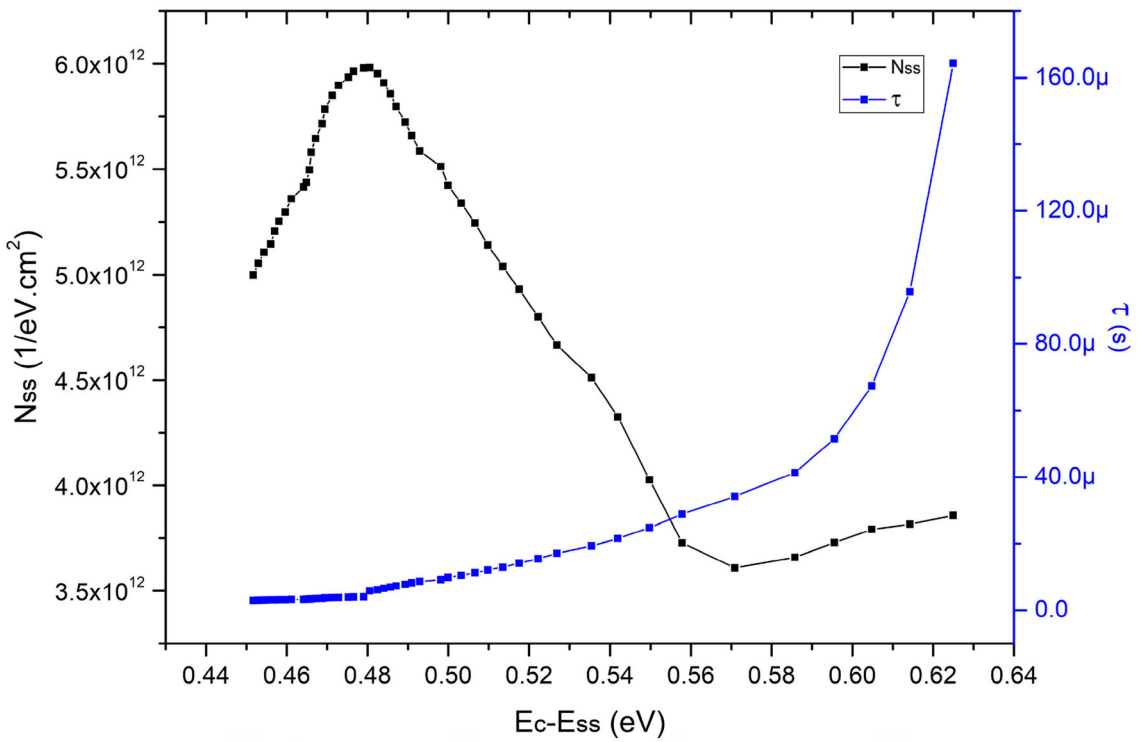

Fig. 10 The surface states (N_{ss}) versus energy level distant from conduction band level (E_c-E_{ss}) of the structure

to 1.98, at the same time the values of N_{ss} for each voltage can be obtained from the peak value of these plots $[N_{ss} = (G_p/\omega)_{max}/(0.402qA)]$. Thus, the N_{ss} values and their relaxation times (τ) were extracted from the peak values of G_p/ω vs $ln(f)$ plots and the frequency, respectively (Fig. 10).

The N_{ss} and τ values were found as 4.999×10^{12}-eV^{-1} cm^{-2} and 2.92 µs at 0.452 eV, and 3.857×10^{12}-eV^{-1} cm^{-2} and 164 µs at 0.625 eV, respectively. In addition, it is clear that the N_{ss} vs E_c-E_{ss} plot has a peak at about 0.48 eV resulting from particular density distribution of surface states depending on relaxation time. E_{ss} is the energy level of the surface states in the forbidden band gap, so E_c–E_{ss} is the energy distance from the conduction band level. Furthermore, the relaxation time τ, increases with rise of E_c–E_{ss} as almost exponentially. The N_{ss} values are on the order of $\sim 10^{12}$ eV^{-1} cm^{-2} and this order is very convenient for any electronic device. The lower N_{ss} values are the consequence of passivation effect of the used NG-PVP polymer interfacial layer.

4 Conclusion

We report that frequency response of C–V–f and G/ω–V–f characteristics of spin-coated nanographite-doped PVP/n-Si structures in a wide frequency (1 kHz–5 MHz) and voltage (± 3 V) ranges at room temperature. The C and G values are strictly dependent on frequency and applied bias voltage and, particularly in the depletion and the accumulation regions due to the effect of N_{ss} and R_s, respectively. The higher values of C and G at low frequency were seen as a consequence of the existence of surface states and their special distribution at interlayer-semiconductor interface. In order to obtain main electrical magnitudes for instance V_D, N_D, E_F, E_m, W_d, and Φ_B were calculated from the intercepts and slopes of C^{-2}–V–f plots as function of frequency. Experimental results show that while the W_d and Φ_B rise with the increase of the frequency, the N_D decreases as almost exponentially. They were found to be strong functions of frequency; N_D, W_d, and Φ_B values change in the ranges of 1.689×10^{15}–7.275×10^{14} cm^{-3}, 0.629–1.457 µm, and 0.745–1.438 eV in a frequency range of 1 kHz to 5 MHz, respectively. The R_s values were also calculated as function of frequency using Nicollian–Goetzberger and they decrease with the increase of the frequency with a nearly exponential characteristic. The energy dependent profile N_{ss} and their τ values were calculated from the conduction method, which were found as 4.999×10^{12} eV^{-1} cm^{-2} and 2.92 µs at 0.452 eV, and 3.857×10^{12} eV^{-1} cm^{-2} and 164 µs at 0.625 eV, respectively. It is evident that these values of N_{ss} are very proper for any electronic device and their lower values are the consequence of the passivation feature of the nanographite-PVP polymer interlayer. In conclusion, the nanographite-PVP polymer layer is candidate instead of insulator/oxide materials such as SiO_2 and SnO_2 prepared with traditional methods such as thermal oxidation owing to its low cost, low molecular weight, high strength electric field, flexibility, and easy production methods such as sol–gel and electrospinning which consume low energy.

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